EXPRESS MAIL LABEL NO.: EV 565664541 US PATENT APPLICATION Docket No: 14993.18 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE application of Greg Scott et al. ) Art Unit Serial No.: 10/611,714 2816 Filed: July 1, 2003 4464 Conf No.: DOUBLE-SIDED EXTENDED DRAIN FIELD For: EFFECT TRANSISTOR, AND INTEGRATED OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION CIRCUIT THAT USES THE SAME Examiner: Anh Quan Tra

## CERTIFICATE OF DEPOSIT UNDER 37 C.F.R. § 1.8

I hereby certify that following documents are being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to: Box: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 28 day of December 2004.

- Transmittal of Issue Fee and Supplemental Declaration (3 pages) (in duplicate)
- PTO Form PTOL-85B transmitting payment of Issue Fee and Publication Fee
- PTO 2038 Credit Card form for \$1,715.00
- Postcard

Respectfully submitted,

Adrian J. Lee

Attorney for Applicant Registration No. 42,785 Customer No. 022913

AJL:ds DS0000002938V001

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Docket No: 14993.18

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of		)
	Greg Scott et al.	)
Serial No.:	10/611,714	) Art Unit ) 2816
Filed:	July 1, 2003	)
Conf No.:	4464	)
For:	DOUBLE-SIDED EXTENDED DRAIN FIELD EFFECT TRANSISTOR, AND INTEGRATED OVERVOLTAGE AND REVERSE VOLTAGE PROTECTION CIRCUIT THAT USES THE SAME	) ) ) )
Examiner:	Anh Quan Tra	)

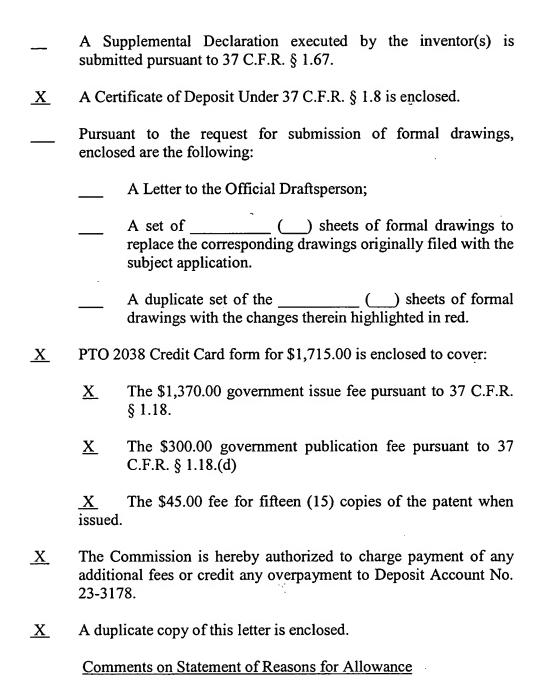
## TRANSMITTAL OF ISSUE FEE PAYMENT

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In response to the Notice of Allowance and Issue Fee Due dated November 23, 2004, please find enclosed herewith the following items for filing in the United States Patent and Trademark Office in connection with the above identified patent application:

X Issue Fee Transmittal (PTOL-85B) submitted pursuant to 37 C.F.R. § 1.311.



On page 2 of the Examiner's Notice of Allowability, the Examiner has indicated that no prior art was found that "Claims 1-20 are allowable because the prior art fails to teach or suggest a circuit (such as figure 1) having a first and second double side extended drain FETs (102,102); and a first resistor R1 coupled

between the power supply and the body terminal of the first double side extended drain FET 102."

Applicants respectfully submit that the claimed invention as set forth in each of the independent claims and the dependent claims must be read as a whole, and not as a single feature or subcombination of features which represent less than the entirety of the claimed invention as a whole. While a particular feature or subcombination of features referred to by the Examiner in the Statement of Reasons for Allowance may represent a basis for distinguishing the claimed invention over the prior art, Applicants further submit that this may not necessarily be the *sole* ground for distinguishing the claimed invention over the prior art of record. Accordingly, the Examiner's statement should, in Applicants' view, not be read as constituting or meaning that the invention can or should be reduced to a single "feature" of the invention or to a subcombination of features that is less than the entire invention claimed as a whole, nor that the single feature referenced by the Examiner or subcombination of features referenced by the Examiner in the Statement of Reasons for Allowance is the only or sole grounds for distinguishing the invention over the prior art of record.

Please address all future correspondence in connection with the aboveidentified patent application to the attention of the undersigned.

Dated this 28th day of December 2004.

Respectfully submitted,

Adrian J. Lee

Attorney for Applicant Registration No. 42,785

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